AMENDMENTS TO THE CLAIMS

1. (Currently amended) A content addressable memory, comprising:

a matchline;

a plurality of content addressable memory cells, coupled to said matchline;

a first current source, coupled to the matchline; and

a second current source, coupled to the matchline;

wherein said first current source is responsive to a first bias current ~~biased~~ to supply a first current to the matchline and to the second current source, and said second current source is responsive to a second bias current ~~biased~~ to supply a second current from the matchline to ground, said first bias current being greater than said second bias current.

2. (Original) The content addressable memory of claim 1, further comprising:

a first current mirror, coupled to said first current source;

a second current mirror, coupled to said second current source; and

a current measurement circuit, coupled to said first current mirror and said second current mirror;

wherein

said first current mirror is coupled to said first current source and configured to supply a third current mirroring said first current to said measurement circuit and said second current mirror, and

said second current mirror is coupled to said second current source and configured to supply a fourth current mirroring said second current.

3. (Original) The content addressable memory of claim 2, wherein said current measurement circuit outputs a voltage reflecting a magnitude of a sense current flowing from said first current source.

4. (Original) The content addressable memory of claim 3, wherein said measurement circuit comprises a first inverter, coupled to said first current mirror and said second current mirror.

5. (Original) The content addressable memory of claim 4, wherein said measurement circuit further comprises:

a second inverter, coupled in series with said first inverter.

6. (Original) The content addressable memory of claim 1, wherein said first current source comprises:

a first transistor, coupled to a power source;

a second transistor, coupled to said first transistor and to the matchline;

wherein said second transistor has a gate terminal coupled to a bias circuit.

7. (Currently amended) The content addressable memory of claim 6, wherein said bias circuit comprises:

a third transistor, coupled to the power source;

a fourth transistor, coupled to said third transistor, and coupled to the gate of said second transistor; and

a first bias current source coupled said fourth transistor and to ground;

wherein said gate of said [[four]] fourth transistor is also coupled to a source/drain terminal of said fourth transistor which is coupled to a terminal of said first bias current source.

8. (Original) The content addressable memory of claim 1, wherein said second current source comprises:

a first transistor, coupled to the matchline;

a second transistor, coupled to said first transistor and to ground;

wherein said first transistor has a gate terminal coupled to a bias circuit.

9. (Original) The content addressable memory of claim 8, wherein said bias circuit comprises:

a second bias current source coupled to a power source;

a third transistor coupled to said second bias current source and coupled to the gate of said first transistor; and

a fourth transistor, coupled to said third transistor and to ground.

10. (Currently amended) A processor based system, comprising:

a processor;

a content addressable memory, coupled to said processor, said content addressable memory comprising:

a matchline;

a plurality of content addressable memory cells, coupled to said matchline;

a first current source, coupled to the matchline; and

a second current source, coupled to the matchline;

wherein said first current source is responsive to a first bias current ~~biased~~ to supply a first current to the matchline and to the second current source, and said second current source is responsive to a second bias current ~~biased~~ to supply a second current from the matchline to ground, said first bias current being greater than said second bias current.

11. (Currently amended) The system of claim 10, further comprising:

a first current mirror, coupled to said first current source;

a second current mirror, coupled to said second current source; and

a current measurement circuit, coupled to said first current mirror and said second current mirror[[;]].

12. (Original) The system of claim 11,

wherein

said first current mirror is coupled to said first current source and configured to supply a third current mirroring said first current to said measurement circuit and said second current mirror, and

said second current mirror is coupled to said second current source and configured to supply a fourth current mirroring said second current.

13. (Original) The system of claim 11, wherein said current measurement circuit outputs a voltage reflecting a magnitude of a sense current flowing from said first current source.

14. (Original) The system of claim 13, wherein said measurement circuit comprises a first inverter, coupled to said first current mirror and said second current mirror.

15. (Original) The system of claim 14, wherein said measurement circuit further comprises:

a second inverter, coupled in series with said first inverter.

16. (Original) The system of claim 10, wherein said first current source comprises:

a first transistor, coupled to a power source;

a second transistor, coupled to said first transistor and to the matchline;

wherein said second transistor has a gate terminal coupled to a bias circuit.

17. (Original) The system of claim 13, wherein said power circuit comprises:

a third transistor, coupled to the power source;

a fourth transistor, coupled to said third transistor and coupled to the gate of said second transistor; and

a first bias current source coupled said fourth transistor and to ground.

18. (Original) The system of claim 10, wherein said second current source comprises:

a first transistor, coupled to the matchline;

a second transistor, coupled to said first transistor and to ground;

wherein said first transistor has a gate terminal coupled to a bias circuit.

19. (Currently amended) The system of claim 18, wherein said bias circuit comprises:

a ~~second~~ bias current source coupled to a power source;

a third transistor coupled to said second bias current source and coupled to the gate of said first transistor; and

a fourth transistor, coupled to said third transistor and to ground.

20. (Original) The system of claim 10, further comprising:

a plurality of network interface devices, each of said network interface devices coupled to said processor, wherein said system routes network traffic between the plurality of network interface devices.

21. (Original) A method for operating a content addressable memory, comprising:

supplying a first current to a matchline;

supplying a second current from said matchline to ground;

wherein said first current is responsive to a first bias current and said second current is responsive to a second bias current, said first bias current being greater than said second bias current.

22. (Currently amended) The method of claim 21, further comprising:

measuring said first current to determine a state of a plurality of CAM cells coupled to said matchline[[;]].

23. (Original) The method of claim 22, wherein said measuring step comprises:

measuring a third current flowing between a first current mirror and a measurement circuit;

wherein a first current mirror is coupled to said first current source and configured to produce the third current, said third current having the same magnitude as said first current.

24. (Original) The method of claim 23, wherein said measuring step indicates that the matchline is in a first logical state when said third current is equal to said first bias current.

25. (Original) The method of clam 24, wherein said measuring step indicates that the matchline is in a second logical state when said third current is equal to said second bias current.